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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,778	08/30/2001	Kunal R. Parekh	4475.1US (98-1097.1)	2586

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EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,778	PAREKH ET AL.	
	Examiner	Art Unit	
	Hoai V Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-10 and 13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-10, 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1,4, 6-9, 10, 13-15, 17-20, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Prall et al. [U.S. Pat. 6,274,423] previously applied, in view of Sandhu et al. [U.S. Pat. 6,124,626] previously applied.

With respect to claims 1, 9-10, and 20, Prall et al. (figures 12-20, cols. 1-8) discloses a DRAM comprising:

a semiconductor substrate (12) having a capacitor structure disposed thereon, the capacitor structure including a storage node (42), a dielectric layer (44) overlying the storage node, and a conductive cell plate (46) overlying the dielectric layer, each of the dielectric layer and the conductive cell plate having an end portion proximate a conductive contact (60), the conductive contact extending downward and adjacently beside the capacitor structure, the end portion of the dielectric layer extending closer to the conductive contact than the end portion of the storage node and the conductive cell plate (see figure 20); and

a doped BPSG layer (56) disposed over the capacitor structure and encasing the end portions of the dielectric layer and the conductive cell plate, the BPSG layer disposed between the capacitor structure and the conductive contact, the conductive contact extending through the BPSG layer (see figure 20).

With respect to claims 4 and 15, Prall et al. discloses that the storage node and the conductive cell plate are heavily doped with dopants (see col. 4, lines 30-32 and lines 42-45).

With respect to claims 6, 7, 17 and 18, Prall et al. discloses that the dielectric layer comprises a capacitor cell dielectric (nitride) layer (see col. 4, lines 41-42).

With respect to claims 8 and 19, Prall et al. discloses that the capacitor structure comprises a container-shaped capacitor (see figure 20).

With respect to claims 9 and 20, Sandhu et al. discloses that the TEOS layer (57) is a dopant barrier (col. 4, lines 54-57) between the capacitor structure and the BPSG (53) (see figure 2).

With respect to claim 13 Prall et al. discloses that the conductive contact comprises at least one of metal (see col. 5, lines 65-67).

With respect to claim 14 Prall et al. discloses that the conductive contact comprises a digit line (62) (see figure 20).

Prall et al. fails to show a TEOS layer disposed between the BPSG layer and the capacitor structure. However, Sandhu et al. shows a TEOS layer (57) disposed between the BPSG layer (53) (col. 3, lines 30-34) and the capacitor structure (48, 50, 52) to wrap around difficult edges or plates (see figures 1-4, col. 6, lines 43-60). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the TEOS layer disposed between the BPSG layer and the capacitor structure as taught by Sandhu et al. in the device of Prall et al. in order to wrap around difficult edges, plates and provide dielectric oxygen loss protection (col. 6, lines 47-50).

4. Claims 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prall et al. [U.S. Pat. 6,274,423] previously applied, and Sandhu et al. [U.S. Pat. 6,124,626] previously applied, as applied to claims 1-4, 6-9, 10-15 and 17-20 above, and further in view of Tsai [U.S. Pat. 5,763,306] previously applied.

Prall et al. substantially discloses the claimed of the DRAM device as discussed in details above except that the storage node and the conductive cell plate are doped with phosphorous. However, Tsai shows that the storage node and the conductive cell plate are doped with phosphorous to increase conductivity (see col. 6, lines 12-22).

Therefore, it would have been obvious to skilled in the art to dope phosphorous in the storage node and the conductive cell plate as taught by Tsai in the device of Prall et al. in order to increase conductivity of the storage node and the conductive cell plate thus increase the capacitance of the capacitor.

Response to Arguments

5. Applicant's arguments filed 3/25/03 have been fully considered but they are not persuasive.

Applicant argues that neither Prall nor Sandhu teach or suggest "a TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and said conductive cell plate, said TEOS layer disposed between said capacitor structure and said conductive contact; and a doped BPSG layer disposed over said TEOS layer, said conductive contact extending through said BPSG layer and said TEOS layer." Applicant's arguments are not persuasive because Sandhu discloses that the TEOS layer (79 of fig. 3; 95 of fig. 4 or 107 of fig. 5) disposed over said capacitor structure (74, 76, 78 of fig. 3; 92, 94, 96 of fig. 4; 114, 116, 107 of fig. 5) and encasing said end portions of said dielectric layer (76 of fig. 3; 94 of fig. 4; 116 of fig. 5) and said conductive cell plate (78 of fig. 3; 96 of fig. 4; 107 of fig. 5). Sandhu also discloses that the doped BPSG layer (53 of fig. 2) disposed over said TEOS layer (57 of fig. 2). In the other hand, Prall discloses that the BPSG layer (56) is disposed between said capacitor structure (42, 44, 46) and said conductive contact (60). Therefore, the combination of Sandhu's reference into the Prall's reference will have the result as

claimed. Specifically, the TEOS layer will be disposed between said capacitor structure and said conductive contact, and the conductive contact will extend through said BPSG layer and said TEOS layer.

Applicant argues that Sandu fails to teach or suggest that region 53 is a BPSG layer. Applicant's arguments are not persuasive because Sandhu discloses that the region 53 (post capacitor formation) is a BPSG layer (see col. 3, lines 30-34).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Sandhu discloses the TEOS layer (57) disposed between the BPSG layer (53) and the capacitor structure (48, 50, 52) to wrap around difficult edges or plates and provide dielectric oxygen loss protection (col. 6, lines 46-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the TEOS layer disposed between the BPSG layer and the capacitor structure as taught by Sandhu et al. in the device of Prall et al. in order to wrap around difficult edges, plates and provide dielectric oxygen loss protection (col. 6, lines 46-50).

Based on what being discussed above, it is concluded that the combination of Sandhu's reference into the Prall's reference disclose every element of the presently claimed invention.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

7. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai V Pham whose telephone number is 703-308-6173. The examiner can normally be reached on 6:30A.M. - 6:00P.M..

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

10. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HP
Hoai Pham
May 21, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800